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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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FAY, SHARPE, FAGAN, MINNICH & MCKEE, LLP
1100 SUPERIOR AVENUE, SEVENTH FLOOR
CLEVELAND, OH 44114

EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,576	DU ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 18-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 18-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the actual individual method steps of claims 1-3, 6, 8, 18-23, & 26 and the specific structural features "a plurality of mesas" (claim 6) and "an insulating material...on sidewalls" (claim 8) must be shown or the features canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. See MPEP § 608.02(p).

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method of manufacturing flip-chip light emitting diode including substrate removal

Pg 8 ln 13 recites "separation of the mesas", however plural mesas are neither depicted in the drawings nor mentioned elsewhere in relevant portions of the specification (pg 5 ln 17, 21, 24; pg 6 ln 26; pg 7 ln 2, 4, 27). Proper antecedent basis should be provided by appropriate amendment to the specification. No new matter should be entered. Plural mesas *per se*, will not be regarded as new matter.

Claim Objections

Claim 21 is objected to because there is insufficient antecedent basis for "the chemical removing" in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7-9, 18-21 and 23-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Shieh (US 5,780,321).

Re claim 1, Shieh discloses method of manufacturing a light emitting diode (col 2 ln 65-67), the method including:

depositing (Fig 2: epitaxially, col 4 ln 47, 55, 60, 64) a plurality of semiconductor layers (16-19) on a deposition substrate (12; col 4 ln 35-36);

removing (Fig 2) at least some of the deposited semiconductor layers (17-20) from a selected trench region of the deposition substrate to define a light-emissive mesa (col 5 ln 61-67);

forming (Fig 2) an electrode (35, col 6 ln 20-22, see Fig 4) on the mesa;

flip-chip bonding (Fig 3, col 7 ln 3-6) the mesa (indirectly) to a first electrical bonding pad (28; col 7 ln 32-34) of a thermally conductive support (25; col 7 ln 4); and

removing the deposition substrate (col 7 ln 67 – col 8 ln 3).

Re claim 7, Shieh discloses (Fig 2) the removing of at least some of the deposited semiconductor layers from a selected trench region includes retaining at least one semiconductor layer (16) that is substantially electrically conductive (col 4 ln 30) in the trench region, and the flip chip bonding further includes:

flip-chip bonding a second electrical bonding pad (another 28) to the retained semiconductor layer in the trench region, wherein the retained semiconductor layer defines an electrical path between the mesa and the second bonding pad (must be, or the LED could not function).

Re claim 8, Shieh discloses (Fig 2) prior to the flip chip-bonding, depositing an insulating material (clear portion on sidewalls must be insulating, or the entire device is shorted and could possibly function) at least on sidewalls of the mesa.

Re claim 9, Shieh discloses the deposition substrate (12) is a GaAs substrate (col 4 ln 35-37), the plurality of semiconductor layers include group III-phosphide layers (col 4 ln 22, ln 47, 54-55, 60, 63-64), and the retained semiconductor layer includes a layer (15) that contains aluminum (col 4 ln 37-39).

Re claim 18, Shieh discloses a method of manufacturing a flip-chip light emitting diode (col 2 ln 65-67), the method including:

epitaxially depositing (Fig 2, col 4 ln 47, 55, 60, 64) semiconductor layers (16-19) that define a light emitting electrical junction on a principle surface of an epitaxy substrate (12; col 4 ln 35-36);

forming (Fig 2) a light-emitting device mesa from the epitaxially deposited semiconductor layers (col 5 ln 61-67);

forming (Fig 2) a first electrode (35, col 6 ln 20-22, see Fig 4) on a portion of the device mesa distal from the epitaxy substrate, the first electrode electrically contacting the device mesa;

disposing (Fig 2) a second electrode (white rectangle directly on top of 16 and to the left of 17) on the principle surface of the substrate;

flip-chip bonding (Fig 3, col 7 ln 3-6) first and second electrodes to bonding pads (28; col 7 ln 32-34);

removing the epitaxy substrate (col 7 ln 67 – col 8 ln 3); and

arranging an electrically conductive, light-transmissive window layer (16, col 4 ln 30-34) over (Fig 2: below) the device mesa and the second electrode, the window layer forming an electrical connection between the device mesa and the second electrode.

Re claim 19, Shieh discloses (Fig 2) the arranging of the window layer includes:

depositing the window layer (16; col 4 ln 46-48) adjacent to the epitaxy substrate during the epitaxial depositing of the semiconductor layers.

Re claim 20, Shieh discloses (Fig 2) disposing of a second electrode on the principle surface of the substrate includes:

forming the second electrode on the window layer, the second electrode electrically contacting the window layer (apparent in Fig 2).

Re claim 21, Shieh discloses the removing of the epitaxy substrate includes:

etching the epitaxy substrate (col 7 ln 67 – col 8 ln 3), wherein the window layer provides (broadest reasonable interpretation: make available) an etch stop (15) for [~~the~~] chemical removing [of said epitaxy substrate].

Re claim 23, Shieh discloses the removing of the epitaxy substrate includes: etching the epitaxy substrate using wet chemical etching (col 8 ln 4-5).

Re claim 24, Shieh discloses the plurality of semiconductor layers (16-19) include group III-phosphide layers (col 4 ln 22, ln 47, 54-55, 60, 63-64).

Re claim 25, Shieh discloses the deposition substrate is a GaAs substrate (12; col 4 ln 35-37).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5, 22, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shieh.

Re claims 2, 22, 26 & 27, Shieh discloses prior to the removing of the deposition substrate, depositing a light-transmissive, electrically conductive window layer (16, col 4 ln 30-34) on a surface of the mesa opposite the (second) electrode, the window layer extending laterally (Fig 2) to electrically contact a second electrical bonding pad (another 28) of the thermally conductive support (25) to define an electrical path between the mesa and the second electrical bonding pad (must be, or the LED could not function). Shieh discloses removing the etch stop layer along with the removing of the deposition substrate (col 8 ln 6-10, col 4 ln 42-46).

Shieh differs from the claimed invention only in not depositing the window layer subsequent to the removing of the deposition substrate.

Shieh teaches the order of method steps may be interchanged (col 8 ln 34-41).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Shieh such that the window layer is formed subsequent to the removing of the deposition substrate; at least to prevent possible damage to the window layer during removal of the deposition substrate (col 8 ln 3-6).

In general, selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. Furthermore, a reference disclosing a particular order of process steps was held to render *prima facie* obvious claims directed to a process of making the same structure by reversing the order of the prior art process steps. See MPEP § 2144.04(IV)(C).

Re claim 3, Shieh as modified above discloses prior to the depositing of a window layer, depositing an insulating material (Fig 2: vertical white portion on sides of 17-19 must be insulating or the entire device is shorted and could not function) between the second electrical bonding pad and the mesa, the window layer extending laterally over (Fig 2: under) the insulating material.

Re claims 4, 5, & 28, Shieh discloses (Fig 2) depositing at least one window layer (16; col 4 ln 46-47). Shieh does not limit his deposition to any particular method (col 8 ln 44-48; clm 1: col 8 ln 52-55; clm 6: col 9 ln 26-30; clm 15: col 10 ln 42-46; clm 22: col 12 ln 3-8), thus the disclosure of Shieh encompasses all well-known deposition types, including liquid phase epitaxy and non-epitaxial deposition (e.g., PVD or CVD).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shieh as respectively applied to claim 1 above, and further in view of Goossen (US 5,923,951).

Re claim 6, Shieh discloses (Fig 2) the removing of at least some of the deposited semiconductor layers to define a light-emissive mesa defines a plurality of mesas (col 5 ln 66-67), and the removing of the deposition substrate effects a physical separation of the mesas (comprising layers 17-19 but not 15-16) in which each mesa is flip-chip bonded to the thermally conductive support (25).

Shieh differs from the claimed invention in not disclosing a plurality of separated light emitting diode device dice.

Goossen teaches it is desirable that removal of semiconductor layers to define mesas is such that removing of the substrate effects a physical separation of the mesas wherein the mesas define a plurality of separated light emitting diode device dice in which each device die is flip-chip bonded to the thermally conductive support (col 3 ln 66 – col 4 ln 3).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Shieh in view of Goossen such that the removing of the deposition substrate effects a physical separation of the mesas wherein the mesas define a plurality of separated light emitting diode dice in which each device die is flip-chip bonded to the thermally conductive support; at least for physical isolation.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shieh as respectively applied to claim 26 above, and further in view of Camras (US 6,784,463).

Re claim 29, Shieh discloses (Fig 2) depositing at least one window layer of GaAs or GaAlP (16; col 4 ln 46-47). Shieh does not limit his deposition to any particular method (col 8 ln 44-48; clm 1: col 8 ln 52-55; clm 6: col 9 ln 26-30; clm 15: col 10 ln 42-46; clm 22: col 12 ln 3-8), therefore the disclosure of Shieh encompasses all well-known deposition types, including liquid phase epitaxy and non-epitaxial deposition (e.g., PVD or CVD). Shieh does teach the window layer must be a good conductor (col 4 ln 50) but does not limit the materials (col 8 ln 44-48; clm 1: col 8 ln 52-55; clm 6: col 9 ln 26-30; clm 15: col 10 ln 42-46; clm 22: col 12 ln 3-8)

Shieh differs from the claimed invention only in not disclosing at least one GaP or AlGaAs window layer.

Camras discloses an analogous group III-Phosphide LED (Fig 4) having a window layer (126) that must have good optical properties and may be selected from various semiconductors (col 8 ln 2-5) including GaP (col 4 ln 64-67).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Shieh in view of Camras such that said window layer is GaP; at least to optimize the device characteristics.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Camras teaches (Fig 4) flip-chip bonding substantially similar to applicant's disclosed arrangement (Fig 2, 5) and the advantages thereof (col 9 ln 25 – col 10 ln 25).

The four Holm et al. patents are incorporated into the disclosure of Shieh (col 5 ln 40-60) and clarify portions thereof not explicitly labeled or shown. For example, US Pat. 5,483,085 discloses (Fig 4-5) the mesa structure of Shieh Fig 2 and clearly labels a first electrode (25; col 3 ln 67), a second electrode (30; col 4 ln 16-17) and an insulating layer (28; col 4 ln 5).

Trezza (US 6,423,560) discloses (Fig 1) flip-chip bonding (col 3 ln 4) of emitters formed on a GaAs substrate (col 2 ln 57-58) including an etch stop (col 2l n 64) used during etch removal of the substrate (col 3ln 13-31).

D'Asaro (US 5,578,162) and Goossen (US 5,385,632) arrays (Fig 7) of flip-chip bonded MQW devices formed on GaAs substrates (Fig 2).

Slater discloses (Fig 2, 4, 5) flip-chip bonding substantially similar to applicant's disclosed arrangement (Fig 2, 5).

Tsukada (US 4,213,805) discloses liquid phase epitaxy applied to light emitting diodes (col 1ln 9-11).

Logan (US 4,464,211) discloses liquid phase epitaxy is well known (col 1 ln 35) and teaches advantages thereof (col 4 ln 5-20). Logan (3,978,426) provides more detailed description of LPE selective growth.

Wolf (Silicon Processing...) teaches that semiconductor thin films may be formed by various methods and that neither PVD nor CVD are necessarily epitaxial (pg 105 ¶1), and that epitaxy occurs only under special conditions (pg 107 ¶6-8).

Goossen (IEEE photon. technol. lett. V.7 N.4) discloses (Fig 1) flip-chip bonding of arrays of LED devices (Fig 4) including substrate removal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571- 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew O Arena
7 November 2006

11/10/06

DOUGLAS W. OWENS
PRIMARY EXAMINER